

SEMICONDUCTOR DEVICE
IN WHICH PUNCHTHROUGH IS PREVENTED

Background of the Invention

5 1. Technical Field

The present invention is relates to a semiconductor device, and more particularly to a semiconductor device in which a device margin is reduced in an input/output protection section.

10 2. Description of the Related Art

Recently, the operation frequency of a semiconductor integrated circuit device becomes very high and a wiring line region allocated for power supply wiring lines and ground wiring lines tends to increase more. Therefore, it becomes easy for an internal circuit of the semiconductor integrated circuit device to result in destruction if a voltage surge is momentary applied or a high voltage is always applied when the semiconductor integrated circuit device is actually used. In order to avoid the destruction of the inner circuit due to application of the voltage surge or the high voltage, a protection circuit is conventionally connected with input/output terminals to improve the voltage endurance of the internal circuit. As one of such techniques, Japanese Laid Open Patent Application (JP-P2002-289704A) describes a technique, in which boron regions of

different depths are formed as P-wells between two N-wells provided in a P-type substrate apart from each other through twice of ion implantation using a same mask, and the deeper boron region is deeper than the
5 two N-wells to increase the breakdown voltage and to suppress leak between the two N-wells at the same time.

However, when the interval between the two N-wells is in order of submicron, it is not possible to
10 keep the breakdown voltage between the two N-wells high in the P-well structure of the above Japanese Laid Open Patent Application (JP-P2002-289704A).

In conjunction with the above description, a semiconductor device is disclosed in Japanese Laid
15 Open Patent Application (JP-A-Heisei 5-267606). In the semiconductor device of this conventional example, a semiconductor substrate of a first conductive type is provided. An embedded layer of a second conductive type opposite to the first conductive type is formed
20 inside the semiconductor substrate over the whole of the semiconductor substrate. A first well of the first conductive type extends from the semiconductor substrate surface into the inside. A wall region of the second conductive type is formed to surround the
25 peripheral of the first well from the embedded layer to the semiconductor substrate surface. A second well of the first conductive type extends from the

semiconductor substrate surface into the inside. A third well of the second conductive type extends from the semiconductor substrate surface into the inside, and is contact with the embedded layer.

5 Also, a semiconductor device is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 6-5867). The semiconductor device of this conventional example is a power MOS transistor formed on a semiconductor substrate of a first conductive type.

10 At lease two well diffusion layers of a second conductive type are provided for the semiconductor substrate to have a predetermined interval. A source region of the first conductive type is formed in the well diffusion layer, and a portion of the

15 semiconductor substrate other than said well diffusion layers is formed as a drain region. A portion of the semiconductor substrate between the two well diffusion layers is of the first conductive type and impurity is doped in a higher concentration in a shallower portion

20 of the semiconductor substrate. A cross section in a horizontal direction becomes larger in a depth direction.

 Also, a semiconductor device is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 2-25 148852). In the semiconductor device of this conventional example, a gate electrode is partially provided on a semiconductor substrate directly or via

a gate insulating film. A drain region and a source region are provided on the gate electrode in the semiconductor substrate surface. An insulating film is provided in a wall region of the drain region other than a lower region below the drain region and a channel region below the gate electrode. An impurity dope region is provided at a predetermined depth straightly below the gate electrode to have the same conductive type as the semiconductor substrate and an impurity concentration higher than that of the semiconductor substrate. The peak impurity concentration position of the impurity dope region is within 0.8 μm from the semiconductor substrate surface.

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Summary of the Invention

An object of the present invention is to provide a semiconductor device, in which it is possible to keep a breakdown voltage between two well regions of a same conductive type high even if the interval between the two well regions is in order of submicrons.

In an aspect of the present invention, a semiconductor device includes a semiconductor region of a first conductive type. First and second regions of a second conductive type opposite to the first conductive type are provided in a surface of the

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semiconductor region in a predetermined interval. A third region of the first conductive type is provided between the first and second regions in the surface of the semiconductor region. A fourth region of the first conductive type is provided below the third region inside the semiconductor region to cover the whole of bottom of the third region at least.

Here, it is desirable that the fourth region is provided below the first to third regions inside the semiconductor region to cover the whole bottoms of the first to third regions.

In this case, a position of an impurity peak concentration of the fourth region into a depth direction is desirably deeper than a peak position of an impurity concentration in each of the first and second regions into the depth direction. More specifically, the position of the impurity peak concentration in the fourth region into the depth direction is desirably deeper in a range of 0.3 to 0.8 μm than that of the impurity peak concentration in each of the first and second regions.

Also, a minimum of the impurity peak concentration of the fourth region is $(1-s) \cdot 1.4\text{E}16$ (atom/cm⁴), where the predetermined interval is s .

Also, the impurity peak concentration of the fourth region becomes higher as the predetermined interval becomes narrower.

Also, the fourth region may be formed by an ion implantation method or by an epitaxial growth method.

5 **Brief Description of the Drawings**

Fig. 1 is a schematic cross sectional view showing a semiconductor device of a first embodiment of the present invention.

Fig. 2 is a diagram showing a potential
10 distribution when a voltage is applied to one of the two N-wells in the semiconductor device of the first embodiment of the present invention.

Fig. 3 is a diagram showing a potential
distribution when a voltage is applied to one of the
15 two N-wells when an embedded P-well is removed from the semiconductor device of the first embodiment of the present invention.

Fig. 4 is a diagram showing a potential
distribution when a voltage is applied to one of the
20 two N-wells when a dose quantity of boron is fixed to $5 \times 10^{12} / \text{cm}^2$ and an ion implantation energy of boron is 300 keV.

Fig. 5 is a diagram showing a potential
distribution when a voltage is applied to one of the
25 two N-wells when a dose quantity of boron is fixed to $5 \times 10^{12} / \text{cm}^2$ and an ion implantation energy of boron is 360 keV.

Fig. 6 is a diagram showing a potential distribution when a voltage is applied to one of the two N-wells when a dose quantity of boron is fixed to $5E12 / \text{cm}^2$ and an ion implantation energy of boron is 400 keV.

Fig. 7 is an impurity distribution of boron when an ion implantation energy of boron is mainly changed and an impurity distribution of the N-well when a dose quantity of phosphor is $2E13 / \text{cm}^2$ and an ion implantation energy is 360 keV for forming the N-wells 2 and 3.

Fig. 8 is a graph showing a minimum necessary interval between the N-well 2 and 3 when the dose quantity of boron is changed by changing an ion implantation energy in a range of 300 to 500 keV.

Fig. 9 is a schematic cross sectional view showing the semiconductor device of a second embodiment of the present invention.

Fig. 10 is a diagram showing a potential distribution when a voltage is applied to one of the two N-wells in the semiconductor device of the second embodiment of the present invention.

Description of the Preferred Embodiments

Hereinafter, a semiconductor device of the present invention will be described with reference to

the attached drawings.

Fig. 1 is a schematic cross sectional view showing the semiconductor device according to the first embodiment of the present invention. In the following description, a P-type semiconductor substrate is used as a semiconductor substrate, two N-wells are provided for the P-type semiconductor substrate and a P-well is provided between them. Also, in the following description, a depletion layer which extends from one of the two N-wells to which a high voltage is applied into the inside of the P-type semiconductor substrate will be described. Therefore, the structure of the surface neighborhood of the P-type semiconductor substrate and the structure on it are omitted in Fig. 1.

As shown in Fig. 1, two N-wells 2 and 3 are first provided for a P-type semiconductor substrate 1, and a P-well 4 is formed between them. A P-well 5 or a P-type epitaxial layer is provided below the two N-wells 2 and 3 and the P-well 4. Trench separation insulating films 6 are provided between the two N-wells 2 and 3 and the P-well 4, and in addition to them, trench separation insulating films 6 are provided in neighborhood with the N-wells 2 and 3 on the opposite side to the P-well 4.

Fig. 2 shows a potential distribution when the P-type semiconductor substrate 1, the N-well 2 and

the P-well 4 are grounded and the voltage of 10 V is applied to the N-well 3 in the above structure. Fig. 3 is a potential distribution when the P-well 5 is not provided in the section structure of Fig. 1.

5 Comparing Fig. 2 and Fig. 3, it could be found that the potential distribution of Fig. 2 is put back within a predetermined depth but the potential distribution of Fig. 3 extends into a down direction and side directions. Thus, it could be understood
10 that the depletion layer from the N-well 3 is put back within the predetermined depth while punchthrough can be prevented in the structure of Fig. 2.

Next, the structure of the P-well 4 will be described. Figs. 4 to 6 show potential distributions
15 when a dose quantity of boron is fixed to $5 \times 10^{12} / \text{cm}^2$ and an ion implantation energy of boron is changed in the range of 300 to 400 keV. The bias condition is the same as the above-mentioned condition.

Fig. 4 is the potential distribution when the
20 ion implantation energy of boron is 300 keV. It could be found that a depletion layer extends downwardly from the N-well 3. It could be considered that because the implantation depth of boron is shallow, the boron is compensated by N-type impurities in the
25 N-well 3 in the lateral direction.

Fig. 5 is the potential distribution when the ion implantation energy of boron is 360 keV. It could

be found that the extension of the depletion layer from the N-well 3 is suppressed.

Fig. 6 is the potential distribution when the ion implantation energy of boron is 400 keV. It could
5 be found that the extension of the depletion layer from the N-well 3 is more suppressed.

When the ion implantation energy of boron is 300 keV as shown in Fig. 4, there is no case where the depletion layer extends from the N-well 3 to the N-
10 well 2 to cause a punchthrough. From the above, it is sufficient that the boron ion implantation energy is 300 keV at minimum, to prevent the punchthrough fully.

Fig. 7 is a diagram showing impurity distributions of boron when the boron ion implantation
15 energy is changed. An impurity distribution in the N-wells 2 and 3 is shown together with the impurity distribution of boron, when phosphor is ion-implanted in a dose quantity of $12E3 /cm^2$ in the ion
implantation energy of 360 keV to form the N-wells 2
20 and 3. The impurity distributions were measured by a secondary ion mass analysis (SIMS).

From the impurity distributions, it could be understood that a boron concentration peak when the boron ion implantation energy is 300 keV is on the
25 position deeper than the phosphor concentration peak of the N-well by about 0.3 micrometers. Also, it could be understood that a boron concentration peak

when the boron ion implantation energy is 500 keV is on the position deeper than the phosphor concentration peak of the N-well by about 0.8 micrometers.

Therefore, a sufficient effect of punchthrough

5 prevention is achieved in the structure of the P-well 4, in which the boron concentration peak is located on a position deeper than the phosphor concentration peak of the N-wells 2 and 3 by about 0.3 to 0.8 micrometers.

10 Next, a relation of the distance between the N-wells 2 and 3 in micrometer and the boron peak concentration is discussed to prevent a punchthrough between the N-wells 2 and 3 sufficiently. It could be understood from Fig. 7 that the boron concentration
15 peak in case of the dose quantity of boron of $1\text{E}12$ / cm^2 and the ion implantation energy of 300 keV and the boron concentration peak in case of the dose quantity of $1\text{E}12$ / cm^2 and the ion implantation energy of 500 keV are approximately same.

20 Fig. 8 is a plot showing the minimum necessary interval between the N-wells 2 and 3 when the ion implantation energy is varied in a range of 300 to 500 keV. Here, the minimum necessary interval
between the N-wells 2 and 3 is defined as the interval
25 in which the punchthrough does not occur even if the voltage of 20 V is applied to the N-well 3 under the above-mentioned bias condition.

When the relation of the minimum necessary interval in micrometer between the N-wells 2 and 3 and the boron peak concentration is approximated by a straight line of the following equation on the logarithm coordinate as show in Fig. 8 by a broken line,

$$n_p = (1-s) \cdot 1.4E16 \text{ (atom/cm}^4\text{)}.$$

Next, the second embodiment of the present invention will be described with reference to the attached drawings. This embodiment differs from the first embodiment in the structure of the P-well and is the same as the first embodiment in the other structure.

As shown in Fig. 9, two N-wells 2 and 3 are provided for the P-type semiconductor substrate 1 and the P-well 4 is put between them. A P-well 15 is provided below the P-well 4 to cover the P-well 4 fully in a plane. For example, trench separation insulating films 6 are provided between the two N-wells 2 and 3 and the P-well 4, and between in the neighborhood of the N-wells 2 and 3 on the opposite side to the P-well 4.

In the above structure, a potential distribution is obtained as shown in Fig. 10 when the P-type semiconductor substrate 1, the N-well 2 and P-well 4 are grounded and the voltage of 10 V is applied to the N-well 3. Comparing the potential distribution

of Fig. 10 and the potential distribution of Fig. 3 in which the P-well 15 is not provided, the 10-V potential line of Fig. 3 extends downwardly and in the lateral direction to the N-well 2, although a 10-V potential line of Fig. 10 is situated between the N-wells 2 and 3 into the lateral direction. It could be understood from this that the extension of the depletion layer from the N-well 3 into the lateral direction is suppressed and the punchthrough can be prevented in the structure of Fig. 9.

Therefore, as understood from the embodiments, if the P-well 15 is provided below the P-well 4 to cover the P-well 4 in a plane at least, the punchthrough between the N-wells 2 and 3 can be prevented.

In the above description, when the P-type epitaxial layer should be provided below the two N-wells and the P-well between them, the P-type epitaxial layer is desirably formed to have the same concentration as that of the above-mentioned well 5 and the same depth as the P-well 5 in the P-type semiconductor substrate.

Also, the present invention is described about the structure in which the two N-wells are provided for the P-type semiconductor substrate, the P-well is provided between them and the embedded P-well is provided below them. However, the

punchthrough between the wells can be prevented and the size reduction of the semiconductor integrated circuit becomes possible by carrying out a similar pattern design and a process design, even in a

5 semiconductor device having the structure of the wells of conductive types opposite to the above conductive types, although the optimal values are different from those described in the embodiments of the present invention.

10 As described above, according to the present invention, by providing the two N-wells for the P-type semiconductor substrate, the P-well between them and the embedded P-well below them, the punchthrough between the wells can be prevented and the interval
15 between the N-wells can be made short.